| INCH-POUND |

MIL-M-38510/507A

26 March 1992
SUPERSEDING
MIL-M-38510/507
12 May 1989

MILITARY SPECIFICATION

MICROCIRCUITS, MEMORY, DIGITAL, CMOS ULTRAVIOLET ERASABLE PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, erasable programmable array logic microcircuits which employ an EPROM cell as the programming element. Two product assurance classes (B and S) and a choice of case outlines and lead finishes are provided and are reflected in the complete Part or Identifying Number (PIN).

1.2 Part or Identifying Number (PIN). The PIN shall be in accordance with MIL-M-38510 (see 3.6 herein).

1.2.1 Device types. The device types shall be as follows:

Device type	Circuit	t_{PD}
01	22-input, 10-output, AND-OR logic array	30 ns
02	22-input, 10-output, AND-OR logic array	25 ns
03	22-input, 10-output, AND-OR logic array	20 ns
04	22-input, 10-output, AND-OR logic array	15 ns

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
K	F-6 (24-lead, .640" x .420" x .090"), flat package; transparent lid to permit UV light erasure
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package; transparent lid to permit UV light erasure
3	C-4 (28-terminal, .460" x .460" x.100"), square chip carrier package; transparent lid to permit UV light erasure

AMSC N/A FSC 5962

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-3.0 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}) 1/	See appendix C, MIL-M-38510
Output voltage applied in high Z state	-0.5 V dc to +7.0 V dc
Output sink current	16 mA
Maximum power dissipation (P_D)	1.2 W
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated copies of federal and military specifications, standards, and handbooks are available from the Standardization Document Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, (except for associated detail specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer-programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this specification.

3.2.3 Logic diagram. The logic diagram for unprogrammed devices shall be as specified on figure 3.

3.2.4 Case outlines. Case outlines shall be in accordance with MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I. The electrical tests for each subgroup are described in table I. Any additional detailed information or electrical test requirements not covered in table I (i.e., pin for pin conditions and testing sequence) shall be maintained and available upon request from the qualifying activity.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.7 Processing EPLD's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.7.1 Erasure of EPLD's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.8.

3.7.2 Programmability of EPLD's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7

3.7.3 Verification of erasure of programmability of EPLDS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Delete the sequence specified in 3.1.9 through 3.1.13 of method 5004 and substitute lines 1 through 5 of table II herein.

b. Burn-in test, method 1015 of MIL-STD-883.

(1) Static test using the circuit shown on figure 4b or equivalent. Ambient temperature (T_A) shall be +125°C minimum. Test duration for the static test shall be 48 hours minimum for class S. The 48-hour burn-in may, at the manufacturer's option, be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic test (test condition D or E) using the circuit shown on figure 4a or equivalent. Test duration and temperature shall be in accordance with method 5004 of MIL-STD-883.

c. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.

d. Post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter measurements.

e. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

f. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 3 may be performed at the wafer level.)

(1) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C, or 2 hours at +300°C for unassembled devices only.

(3) Perform margin test using V_m = +5.7 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2b.(2)).

(5) Perform margin test using V_m = +5.7 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(6) Perform electrical tests (see 4.2c).

(7) Erase (see 3.7.1). Devices may be submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.7.3).

The maximum unbiased bake temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7 and 8 shall be by attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies a device type, then the slower device types of the same die type (see MIL-M-38510, 3.1.3.21) may be part I qualified upon the request of the manufacturer, without any further testing.

4.3.2 Electrostatic discharge sensitivity (ESDS). ESDS testing shall be performed in accordance with MIL-STD-883, method 3015 for initial testing and after any design or process changes which may affect input-output protection circuitry. The option to categorize devices as ESD sensitive without performing the test is not allowed.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

a. Class S devices selected for testing in subgroup 5 (table IIa of method 5005 of MIL-STD-883) shall be programmed in accordance with 3.2.2 herein.

b. Electrical parameters shall be as specified in table II herein.

c. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883 using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 4 or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical tests shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D or E, using the circuit shown on figure 4, or equivalent.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) The devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical tests shall be as specified in table II herein.

b. The devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed. After completion of all testing, the devices shall be erased and verified.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of packaging. The sampling and inspection of the preservation, packing and container marking shall be in accordance with the requirements of MIL-M-38510.

4.7 Programming procedure. The programming specifications on figure 6, figure 7, in table III, table IV, table V, table VI, table VII, table VIII, and the following procedures shall be used for programming the device:

a. Initially and after each erasure, all cells, with the exception of the security bit, are in the "0" state. A "1" indicates that an unprogrammed location is to be programmed and a "0" indicates that an unprogrammed location is to remain unprogrammed. All locations to be programmed are addressed as row and column locations. Table V through table VIII provide the specific address for each addressed location to be programmed.

b. The programming flow chart on figure 7 describes the sequence of operations for programming the Normal and Phantom arrays, the Normal and Phantom Output Enable product terms, the Set and Preset product terms, the Top Test product term, the Bottom Test product term, and the Architecture bits. The sequencing and timing of the signals is shown on figure 6a. All setup, hold, and delay times must be met, and the sequence of operations should be strictly followed. Proper sequencing of all power and supervoltages is essential for reliable programming of the device.

c. After all locations are programmed, a verify of all words is required as shown on figure 6. When performing this verify only operation, eliminate the program portion of the cycle but maintain the setup and hold timing relative to the verify pulse. Under no circumstances should the verify signal be held low and the addresses toggled as it violates address setup and hold times. The overprogram pulse in step 10 of figure 7 is a variable, "4" times the initial value when programming the Normal, Phantom, Top Test, Bottom Test and Output Enable product terms and "8" times the initial value when programming the Architecture bits.

d. The security cell is programmed per figure 6b with a single 50 ms pulse on I_{11}. A supervoltage on I_3 is used to verify the security cell after V_{PP} has been removed from I_0. Data in is represented as a supervoltage on I_2 and verified as a TTL signal output on the same pin. A "0" on I_2 indicates that the security bit has been programmed, and a "1" indicates that the security has not been programmed.

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Test conditions T_C = -55°C to +125°C	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.0 V V_{IH} = 5.0 V, I_{OH} = -2.0 mA	1, 2, 3 (3006)	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.0 V V_{IH} = 5.0 V, I_{OL} = 12.0 mA	1, 2, 3 (3007)	All		0.5	V
Input high level 1/ voltage	V_{IH}	V_{CC} = 4.5 V	1, 2, 3 (3008)	All	2.0		V
Input low level 1/ voltage	V_{IL}	V_{CC} = 4.5 V	1, 2, 3 (3008)	All		0.8	V
High impedance output leakage current 2/	I_{OZL}	V_{CC} = 5.5 V, V_{IL} = 0.0 V V_{IH} = 5.0 V, V_O = 0.0 V	1, 2, 3 (3020)	All	-40		µA
High impedance output leakage current 2/	I_{OZH}	V_{CC} = 5.5 V, V_{IL} = 0.0 V V_{IH} = 5.0 V, V_O = 5.5 V	1, 2, 3 (3021)	All		40	µA
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IH} = 5.5 V	1, 2, 3 (3010)	All		10	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IL} = 0.0 V	1, 2, 3 (3009)	All	-10		µA
Supply current	I_{CC}	V_{CC} = 5.5 V I/O = open Pins (I_0-I_{11}) = 0.0 V	1, 2, 3 (3005)	All		120	mA
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V, V_O = 0.5 V	1, 2, 3 (3011)	All	-30	-90	mA
Input capacitance 4/	C_I	V_{CC} = 5.0 V, V_I = 0.0 V T_C = +25°C, f = 1 MHz (see 4.4.1d)	4 (3012)	All		10	pF
Output capacitance 4/	C_O	V_{CC} = 5.0 V, V_O = 0.0 V T_C = +25°C, f = 1 MHz (see 4.4.1d)	4 (3012)	All		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions T_C = -55°C to +125°C	Group A subgroups (test method)	Device types	Limits Min	Limits Max	Unit
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V See figure 5	9, 10, 11	01		30	ns
				02		25	
			(3003)	03		20	
				04		15	
Clock to output 5/	t_{CO}		9, 10, 11	01		20	ns
				02		15	
			(3003)	03		15	
				04		10	
Input to output enable	t_{PZH}		9, 10, 11	01		25	ns
				02		25	
			(3003)	03		20	
				04		15	
Input to output enable	t_{PZL}		9, 10, 11	01		25	ns
				02		25	
			(3003)	03		20	
				04		15	
Input to output disable	t_{PHZ}		9, 10, 11	01		25	ns
				02		25	
			(3003)	03		20	
				04		15	
Input to output disable	t_{PLZ}		9, 10, 11	01		25	ns
				02		25	
			(3003)	03		20	
				04		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions T_C = -55°C to +125°C	Group A subgroups (test method)	Device types	Limits Min	Limits Max	Unit
Clock pulse width 4/	t_{WH}	V_{CC} = 4.5 V See figure 5	9, 10, 11	01	20		ns
				02	15		
			(3003)	03	15		
				04	6		
Clock pulse width 4/	t_{WL}		9, 10, 11	01	20		ns
				02	15		
			(3003)	03	15		
				04	6		
Setup time	t_S		9, 10, 11	01	20		ns
				02	18		
			(3003)	03	17		
				04	12		
Hold time	t_H		9, 10, 11 (3003)	All	0		ns
Maximum clock frequency 6/	f_{MAX}		9, 10, 11	01	25		MHz
				02	30		
			(3003)	03	31.2		
				04	45		
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01	30		ns
				02	25		
			(3003)	03	20		
				04	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions T_C = -55°C to +125°C	Group A subgroups (test method)	Device types	Limits Min	Limits Max	Unit
Asynchronous reset recovery time	t_{AR}	V_{CC} = 4.5 V See figure 5	9, 10, 11	01	30		ns
				02	25		
			(3003)	03	20		
				04	15		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01		30	ns
				02		25	
			(3003)	03		25	
				04		20	

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3/ For test purposes, not more than one output should be shorted at a time. Short circuit test duration should not exceed one second.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ Test applies only to registered outputs.
6/ f_{MAX} is derived by testing t_S and t_{CO} and is not tested directly. $f_{MAX} = 1/(t_S + t_{CO})$.

TABLE II. Burn-in and electrical test requirements.

Line no.	Applicable tests and MIL-STD-883 test method	Class S devices 1/ 2/			Class B devices 1/ 2/		
		Reference paragraph	Table I 3/ subgroups	Table IX delta 4/ limits	Reference paragraph	Table I 3/ subgroups	Table IX delta 4/ limits
1	Interim electrical parameters (method 5004)		1			1	
2	Static burn-in I (method 1015)	4.2b	Required				
3	Same as line 1		1*	Δ			
4	Static burn-in II (method 1015)	4.2b	Required				
5	Same as line 1		1*	Δ			
6	Dynamic burn-in (method 1015)	4.2b	Required		4.2b	Required	
7	Same as line 1	4.2d	1*				
8	Final electrical parameters (method 5004)		1*,2,3,7,8, 9,10,11 5/	Δ		1*,2,3,7,8, 9,10,11	
9	Group A test requirements (method 5005)	4.4.1	1,2,3,7,8, 9,10,11		4.4.1	1,2,3,7,8, 9,10,11	
10	Group B end-point electrical parameters (method 5005)	4.4.2	1,2,3,7,8, 9,10,11	Δ			
11	Group C end-point electrical parameters (method 5005)				4.4.3	1,2,3,7,8 5/ 6/	Δ
12	Group D end-point electrical parameters (method 5005)	4.4.4	1,2,3,7,8		4.4.4	1,2,3,7,8	

1/ Blank spaces indicate tests are not applicable.
2/ For subgroups 9, 10, and 11 only the worst value measured per device need be recorded when variables data is required (e.g., during qualification).
3/ * indicates PDA applies to subgroup 1 (see 4.2e).
4/ Δ indicates delta limit shall be required only on table IX, subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1). Refer to table IX for required parameters and limits to be tested.
5/ The device manufacturer may at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).
6/ For class B, delta limits shall be required on initial qualification or after any design changes which may affect the parameters listed in table IX. Delta values shall be computed with reference to the previous interim electrical parameters.

Device types	01, 02, 03, and 04	
Case outlines	K, L	3
Terminal number	Terminal symbol	
1	CP/I_0	NC
2	I_1	CP/I_0
3	I_2	I_1
4	I_3	I_2
5	I_4	I_3
6	I_5	I_4
7	I_6	I_5
8	I_7	NC
9	I_8	I_6
10	I_9	I_7
11	I_{10}	I_8
12	GND	I_9
13	I_{11}	I_{10}
14	I/O_0	GND
15	I/O_1	NC
16	I/O_2	I_{11}
17	I/O_3	I/O_0
18	I/O_4	I/O_1
19	I/O_5	I/O_2
20	I/O_6	I/O_3
21	I/O_7	I/O_4
22	I/O_8	NC
23	I/O_9	I/O_5
24	V_{CC}	I/O_6
25	---	I/O_7
26	---	I/O_8
27	---	I/O_9
28	---	V_{CC}

FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
$CP\backslash I_0$	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	I/O_8	I/O_9
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = High impedance
2. X = Don't care

FIGURE 2. Truth table (unprogrammed).

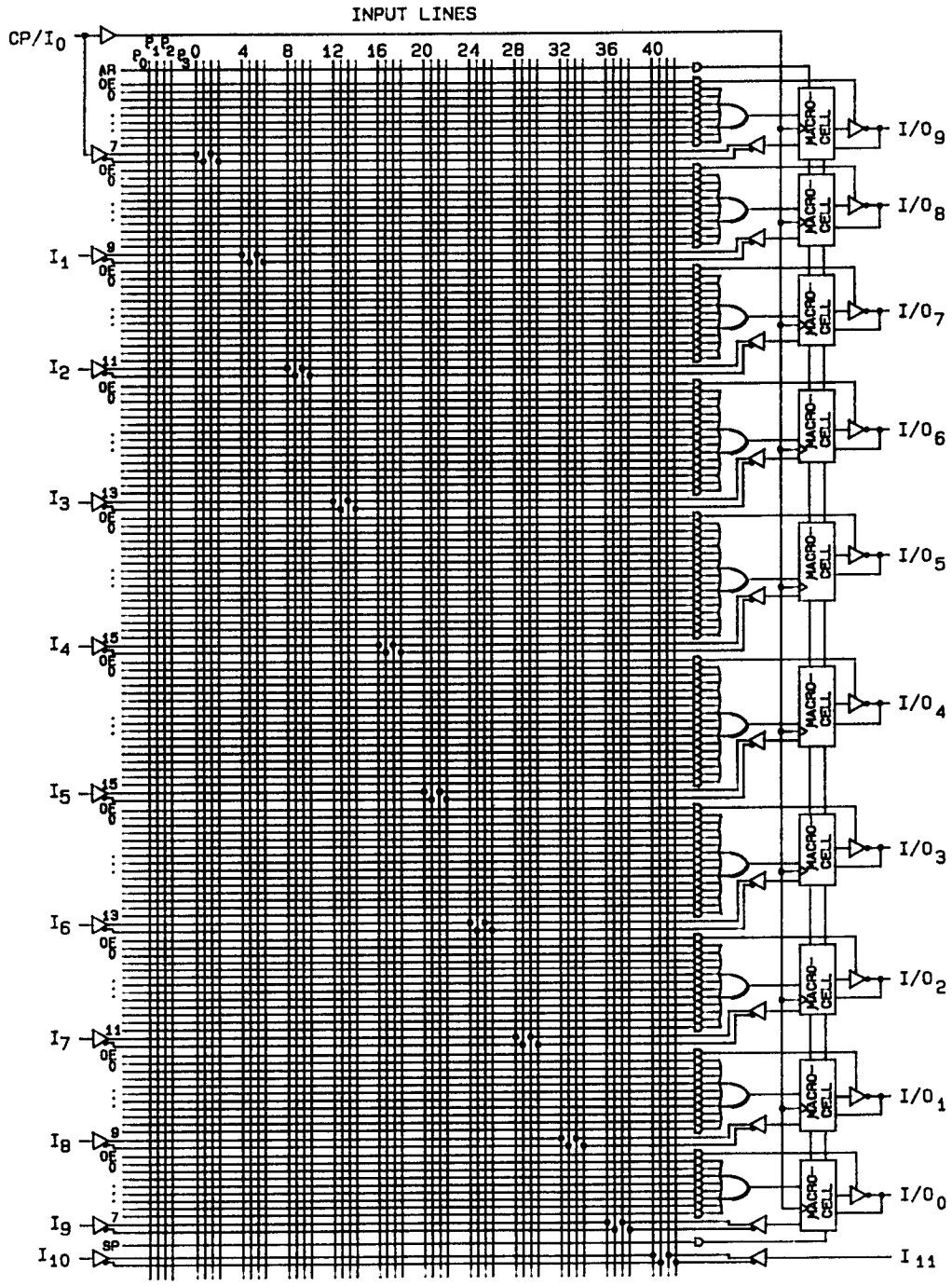


FIGURE 3. Logic diagram (unprogrammed).

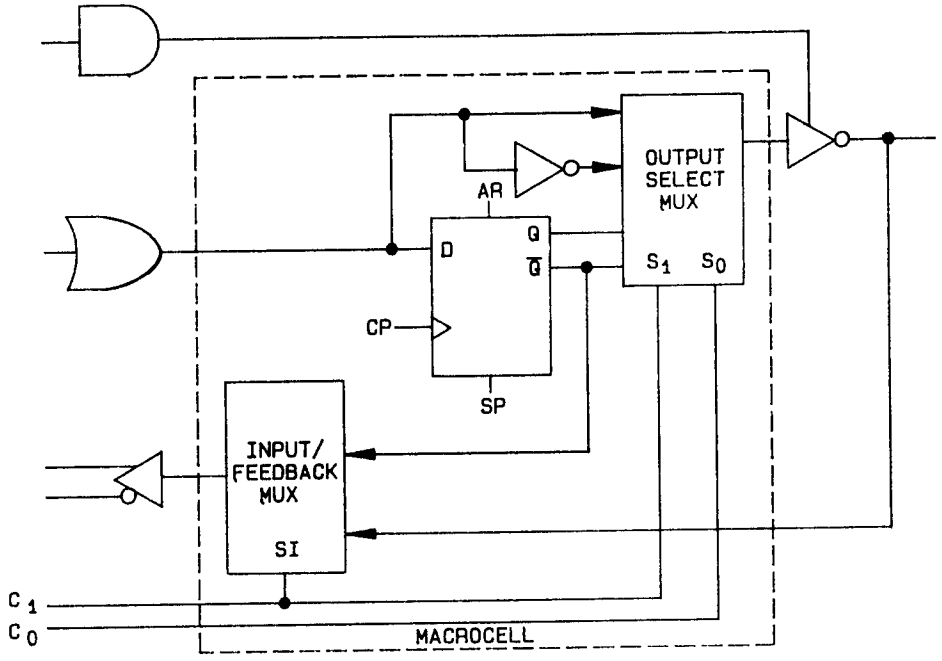
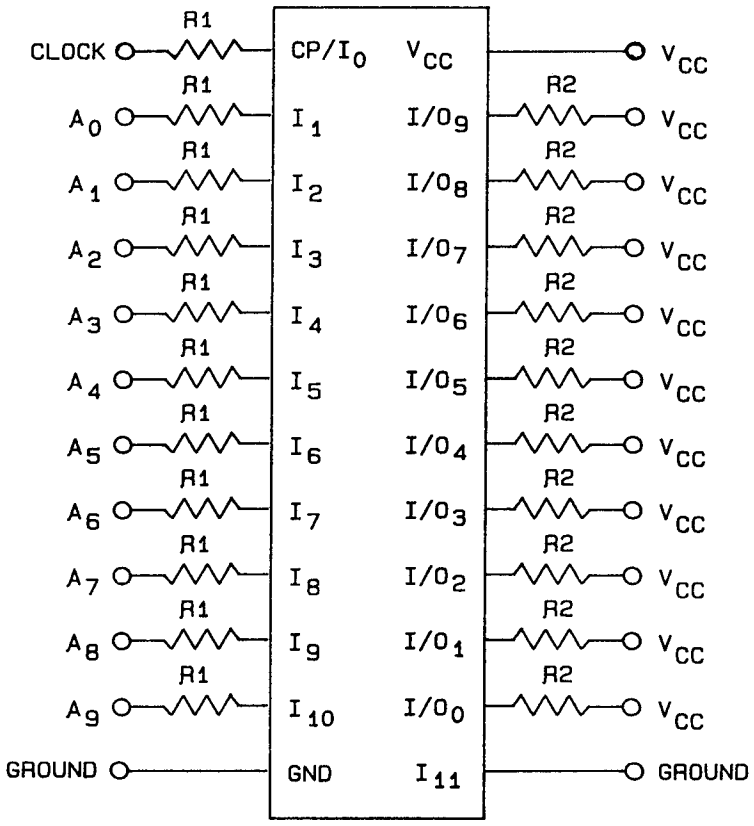


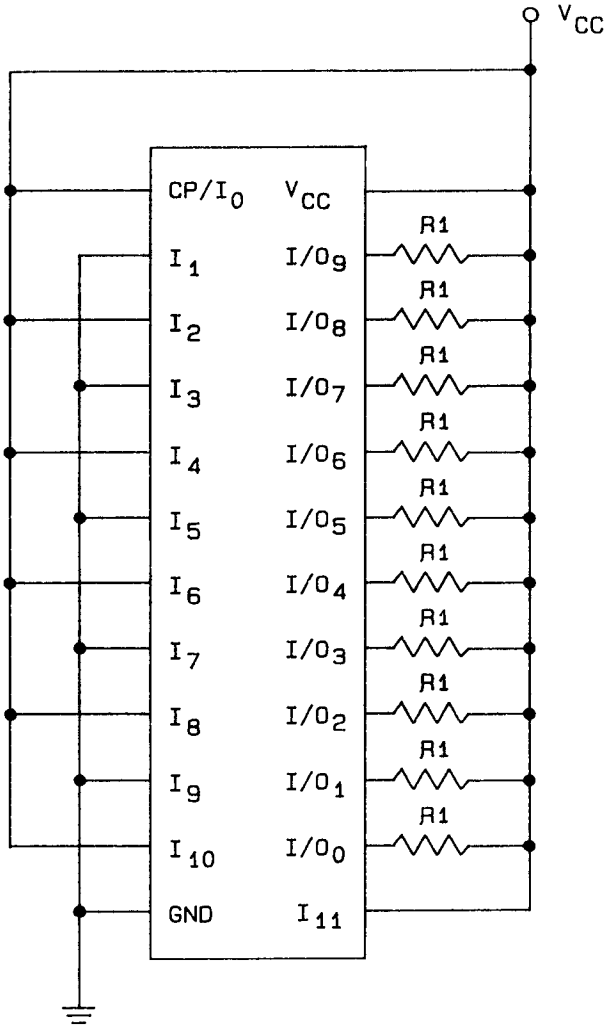
FIGURE 3. Logic diagram (unprogrammed) - Continued.



NOTES:
1. R1 = 1 kΩ ±5% and is located on the program board. Each R1 feeds a maximum of 420 devices.
2. R2 = 1 kΩ ±5% and is located at each device pin.
3. There is one 0.1 μF decoupling capacitor on every socket between V_{CC} and ground.
4. All pulse generators have the following characteristics:
   V_{IL} = -0.25 V minimum to 0.25 maximum; V_{IH} = 2.75 V minimum to 3.25 V maximum.
5. V_{CC} = 5.75 V ±0.25 V.
6. Input frequencies are as follows:

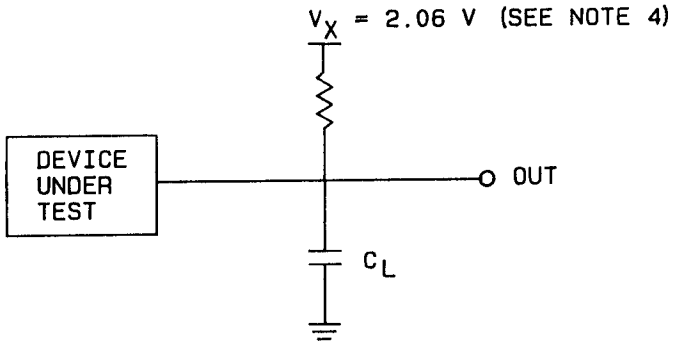
Input	Frequency(±50%)	Input	Frequency (±50%)
CLOCK	f_0 = 500 kHz	A_5	$f_6 = 1/64\ f_0$
A_0	$f_1 = 1/2\ f_0$	A_6	$f_7 = 1/128\ f_0$
A_1	$f_2 = 1/4\ f_0$	A_7	$f_8 = 1/256\ f_0$
A_2	$f_3 = 1/8\ f_0$	A_8	$f_9 = 1/512\ f_0$
A_3	$f_4 = 1/16\ f_0$	A_9	$f_{10} = 1/1024\ f_0$
A_4	$f_5 = 1/32\ f_0$		

FIGURE 4a. Burn-in and life test circuit.



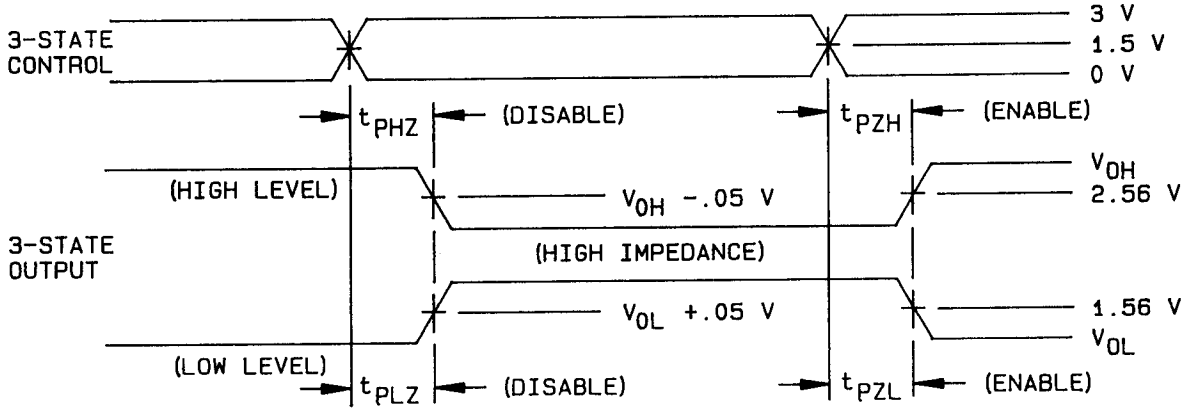
NOTES:
1. R1 = 1Ω ±5%.
2. V_{CC} = 6.50 V ±0.25 V.
3. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC} and V_{CC} to V_{SS}).

FIGURE 4b. Static burn-in circuit.



NOTES:
1. C_L = 50 pF minimum, including jig and probe capacitance. t_{PHZ} and t_{PLZ} are specified with C_L = 5 pF. R1 = 105 ohms ±1 percent.
2. Outputs may be under load simultaneously.
3. V_{IH} = 3.0 V, V_{IL} = 0.0 V.
4. For t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}:

Test	V_X	Output measurement level
t_{PHZ}	2.06	2.56 V
t_{PZL}	2.06	1.56 V
t_{PHZ}	1.5	V_{OH} -0.5 V
t_{PLZ}	2.60	V_{OL} +0.5 V



OUTPUT CONTROL SWITCHING WAVEFORM

FIGURE 5. Switching time test circuit and waveforms.

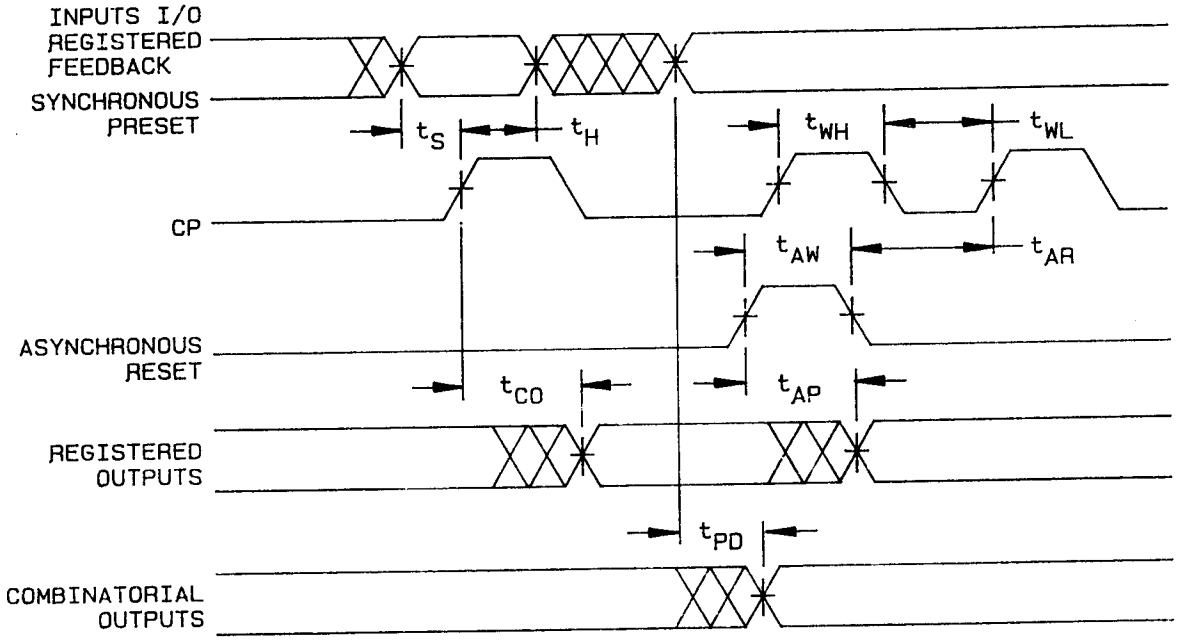
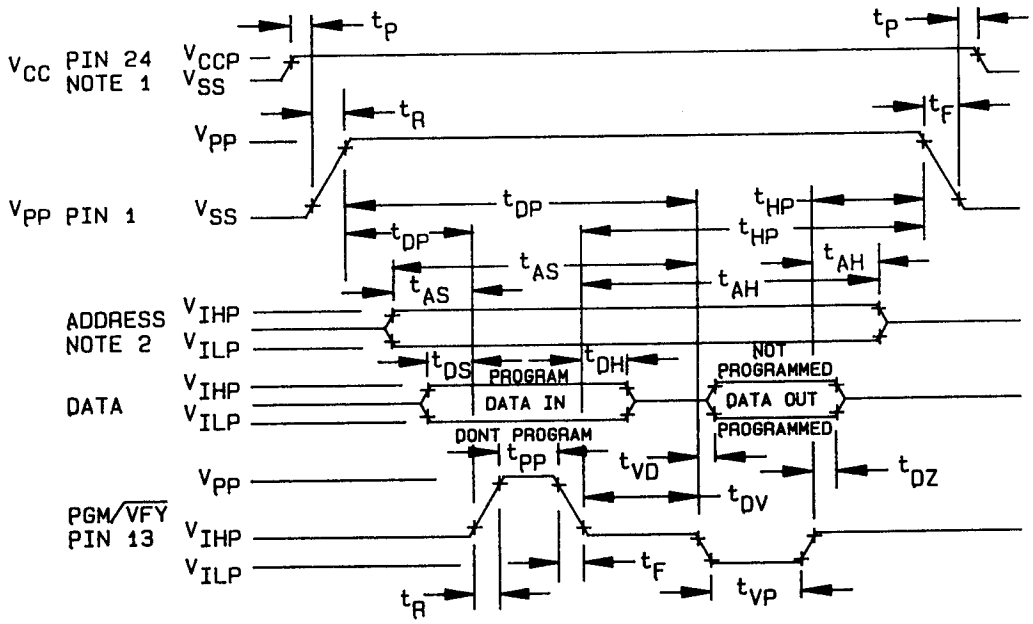


FIGURE 5. Switching time test circuit and waveforms - Continued.



NOTES:
1. Power, V_{PP} and V_{CC} should not be cycled for each program/verify cycle, but may remain static during programming.
2. For programming $\overline{OE}$ Product Terms and Architecture bits, pin 11 (A9) must go to V_{PP} and satisfy t_{AS} and t_{AH}.

FIGURE 6a. Programming waveforms.

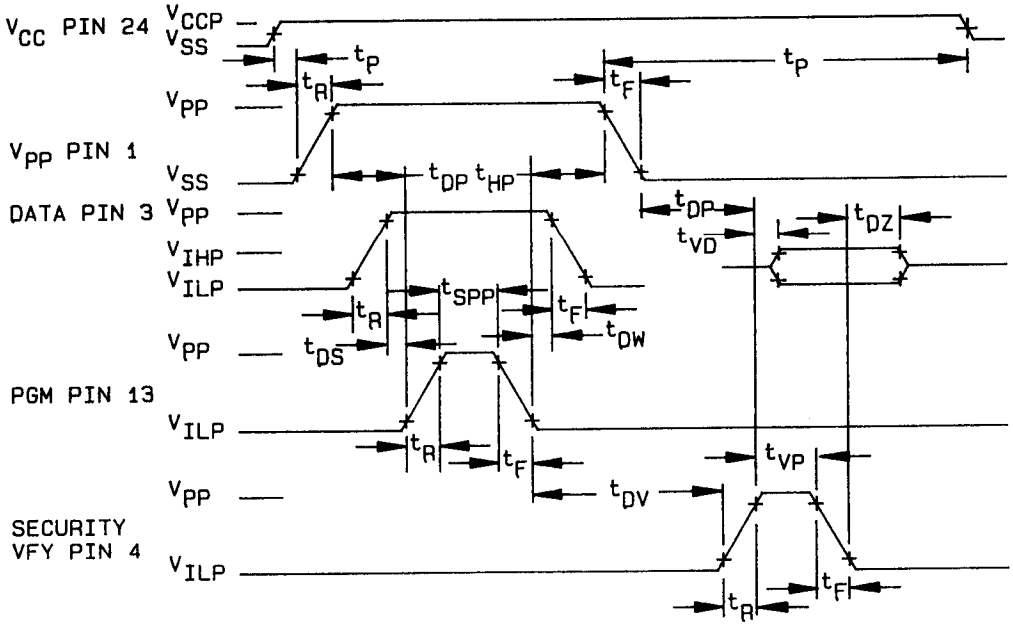
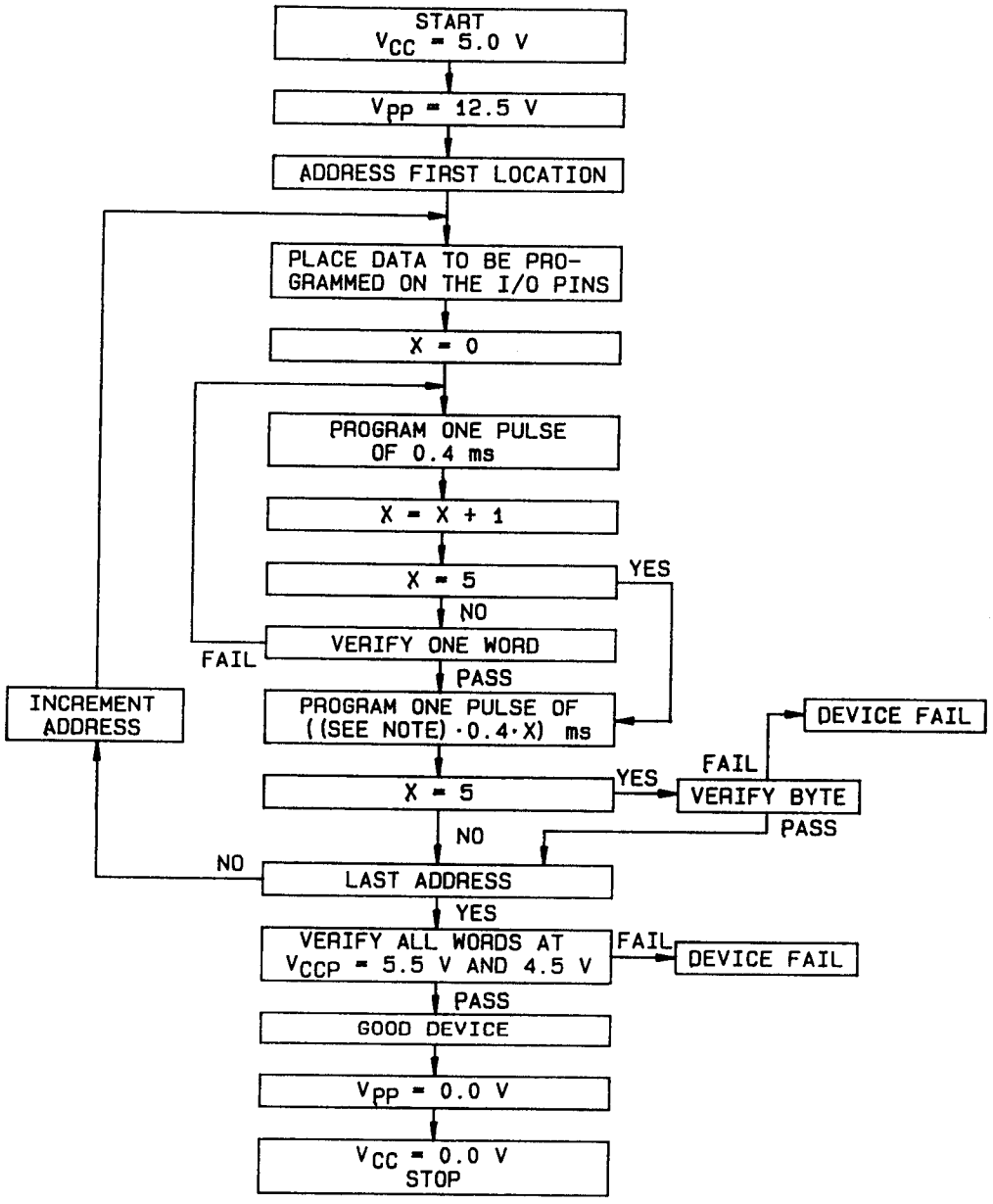


FIGURE 6a. Programming waveforms for security cell.



NOTE: This value is "41" for programming the NORMAL array, PHANTOM array TOP TEST, BOTTOM TEST and OUTPUT ENABLE PRODUCT TERMS. The value is "8" when programming ARCHITECTURE BITS.

FIGURE 7. Programming flowchart.

TABLE III. Operating modes. 1/

Feature	Mode	Pin identification																
		CPI_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	IO_0	IO_3	IO_6	IO_1IO_2 IO_4IO_5 IO_7IO_8	IO_9
Main Array Product	Program	PP	Table V						Table VI				PP	Data In				
	Inhibit	PP											HP	High Z				
	Verify 2/	PP											LP	Data out				
OE Product Terms	Program	PP	Table V						HP	HP	HP	PP	PP	Data In				
	Inhibit	PP							HP	HP	HP	PP	HP	High Z				
	Verify	PP							HP	HP	HP	PP	LP	Data out				
SyncSet Async 3/ Reset TopTest BotTest	Program	PP	Table V						HP	HP	HP	HP	PP	Data In	Data In	Data In	LP	Data In
	Inhibit	PP							HP	HP	HP	HP	HP	Z	Z	Z	Z	Z
	Verify	PP							HP	HP	HP	HP	LP	Data Out	Data Out	Data Out	Driven	Data Out
Architecture Bits	Program	PP	HP	HP	HP	HP	HP	HP	LP	Table VII		PP	PP	Data In				
	Inhibit	PP	HP	HP	HP	HP	HP	HP	LP			PP	HP	High Z				
	Verify	PP	HP	HP	HP	HP	HP	HP	LP			PP	LP	Data out				
Security Bit	Program	PP	LP	PP	LP	LP	LP	LP	LP	LP	LP	LP	PP	LP	LP	LP	LP	LP
	Verify	LP	LP	Data Out	PP	LP	LP	LP	LP	LP	LP	LP	LP	Driven Outputs				
PAL Mode Operatn	Normal	CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O				
	Phantom	NA	I	NA	NA	NA	PP	I	NA	NA	I	I	NA	Output				
	TopTest	I	I	I	I	I	I	I	I	PP	I	I	I	NA				Out
	BotTest	I	I	I	I	I	I	I	I	I	PP	I	I	Out	NA			
	RPreld	4/	NA	NA	NA	NA	NA	NA	PP	NA	NA	NA	LP	Data In				
Phantom Array P Terms	Program	PP	LP	LP	Table VIII		LP	PP	Table VI				PP	Data In				
	Inhibit	PP	LP	LP			LP	PP					HP	High Z				
	Verify	PP	LP	LP			LP	PP					LP	Data Out				
Phantom OE P Terms	Program	PP	LP	LP	Table VIII		LP	PP	HP	HP	HP	PP	PP	Data In				
	Inhibit	PP	LP	LP			LP	PP	HP	HP	HP	PP	HP	High Z				
	Verify	PP	LP	LP			LP	PP	HP	HP	HP	PP	LP	Data Out				

See footnotes at end of table.

TABLE III. Operating modes. 1/

1/ Voltage legend:

LP = Low level input programming voltage (V_{ILP}).
HP = High level input programming voltage (V_{IHP}).
PP = Program voltage (V_{PP}).
Z = High impedance.

2/ It is necessary to toggle $\overline{OE}$ (I_{11}) high during all address transitions while in the program verify/blank check mode.

3/ Data In and Data Out for programming Synchronous Set, Asynchronous Reset, Top Test and Bottom Test is programmed and verified on the following pins:
I/O_0 = Bottom Test
I/O_3 = Synchronous Set
I/O_6 = Asynchronous Reset
I/O_9 = Top Test

4/ The preload clock on CP/I_0 loads the Registers on a low going high transition.

TABLE IV. Programming characteristics.

Parameter	Symbol	Conditions T_A = +25°C ±5°C	Device types	Limits		Unit
				Min	Max	
Programming voltage	V_{PP}		All	12.0	13.0	V
Supply voltage during programming	V_{CCP}		All	4.75	5.25	V
Input high voltage during programming	V_{IHP}		All	3.0	V_{CCP}	V
Input low voltage during programming	V_{ILP}		All	-3.0	0.4	V
Output high voltage	V_{OH}		All	2.4		V
Output low voltage	V_{OL}		All		0.4	V
Programming supply current	I_{PP}		All		40	mA
Delay to programming voltage	t_P		All	20		ms
Delay to program	t_{DP}		All	1		µs
Hold from program or verify	t_{HP}		All	1		µs

TABLE IV. Programming characteristics - Continued.

Parameter	Symbol	Conditions T_A = +25°C ±5°C	Device types	Limits		Unit
				Min	Max	
V_{PP} rise and fall time	$t_{R,F}$		All	50		ns
Address setup time	t_{AS}		All	1		µs
Address hold time	t_{AH}		All	1		µs
Data setup time	t_{DS}		All	1		µs
Data hold time	t_{DH}		All	1		µs
Programming pulse width	t_{PP}		All	0.4	10	ms
Programming pulse width for security	t_{SPP}		All	50		ms
Delay from program to verify	t_{DV}		All	2		µs
Delay to data out	t_{VD}		All		1	µs
Verify pulse width	t_{VP}		All	2		µs
Verify to high Z	t_{DZ}		All		1	µs

TABLE V. Input term addresses.

Input term	Pin name					
	I_1	I_2	I_3	I_4	I_5	I_6
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
8	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
9	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
11	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
12	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
13	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
15	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
16	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
18	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
19	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
20	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
22	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
23	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
24	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
25	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
26	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
28	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
29	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
30	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
32	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
33	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
34	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
35	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
36	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
37	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
38	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
39	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
40	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
41	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
42	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
43	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}

TABLE VI. Product term addresses.

Product term	Pin name			
	I_7	I_8	I_9	I_{10}
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
8	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
9	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
11	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
12	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
13	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
15	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}

TABLE VII. Architecture bit addressing.

Architecture bit	I_8	I_9
Output polarity (C_0)	V_{ILP}	V_{ILP}
Register/Nonregister output (C_1)	V_{IHP}	V_{ILP}

TABLE VIII. Phantom input term addresses.

Phantom input term	I_3	I_4
P_0	V_{ILP}	V_{ILP}
P_1	V_{IHP}	V_{ILP}
P_2	V_{ILP}	V_{IHP}
P_3	V_{IHP}	V_{IHP}

TABLE IX. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC}	±2 mA
I_{OZH}	±10% of specified value
I_{OZH}	±10% of specified value

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

4.8 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (A). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for use for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. Acquisition documents should specify the following:

a. Complete Part or Identifying Number (PIN) (see 1.2).

b. Requirement for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirement for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special lead lengths or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

h. Requirements for programming the device, including processing option.

i. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND - - - - - - - - - - - - - Ground zero voltage potential.

V_{IN} - - - - - - - - - - - - Voltage level at an input terminal.

I_{IN} - - - - - - - - - - - - Current flowing into an input terminal.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the PIN. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use of quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Vendor similar part number
01	C22V10-30
02	C22V10-25
03	C22V10-20
04	C22V10-15

6.6 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiviness of the changes.

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1251)